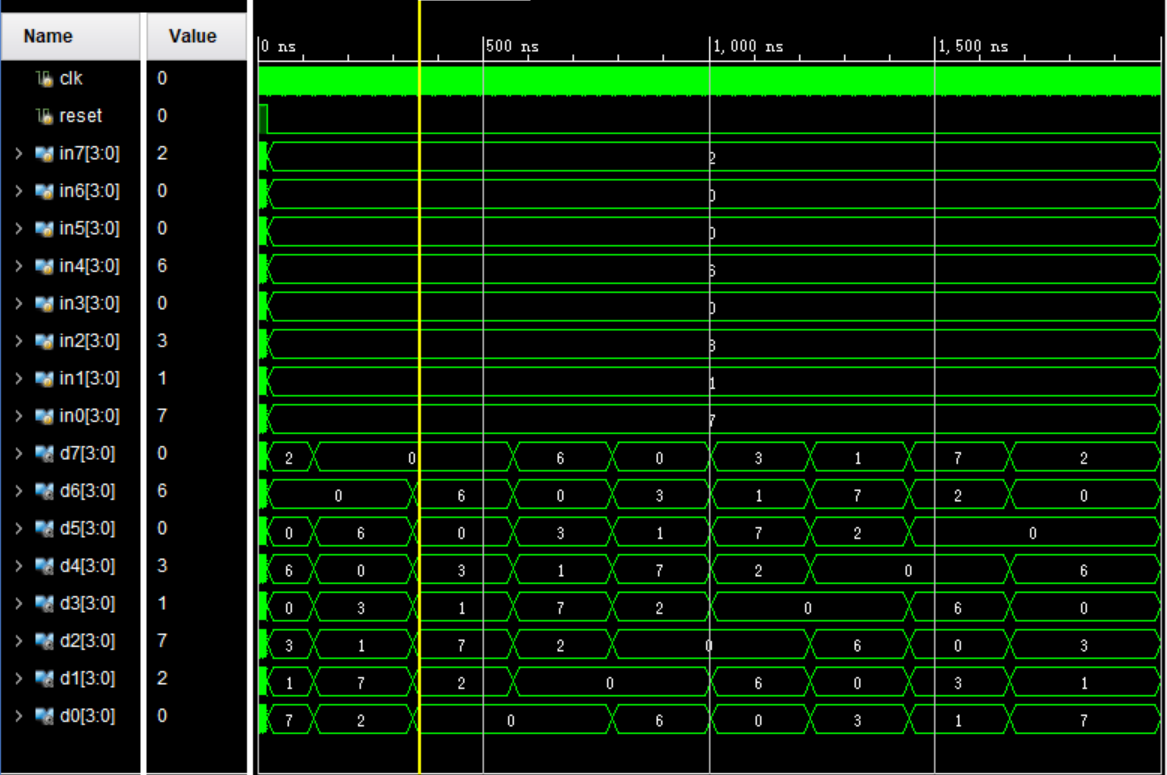
**实验报告 Lab 5**

一、行为级代码（见附页）

二、仿真

八位输入：20060317



三、板子现象

八位输入：20250326

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|  |  |

**附页** 行为级代码

module str\_display(

input clk,

input reset,

output [3:0]an1,

output [3:0]an0,

output a1,

output b1,

output c1,

output d1,

output e1,

output f1,

output g1,

output a0,

output b0,

output c0,

output d0,

output e0,

output f0,

output g0

);

wire [3:0]di7;

wire [3:0]di6;

wire [3:0]di5;

wire [3:0]di4;

wire [3:0]di3;

wire [3:0]di2;

wire [3:0]di1;

wire [3:0]di0;

roll roll1 (

.clk(clk),

.reset(~reset),

.in7(2),

.in6(0),

.in5(2),

.in4(5),

.in3(0),

.in2(3),

.in1(2),

.in0(6),

.d7(di7),

.d6(di6),

.d5(di5),

.d4(di4),

.d3(di3),

.d2(di2),

.d1(di1),

.d0(di0)

);

display

dis1(.clk(clk),.reset(1),.in3(di7),.in2(di6),.in1(di5),.in0(di4),.an(an1),.a(a1),.b(b1),.c(c1),.d(d1),.e(e1),.f(f1),.g(g1));

display dis0(.clk(clk),.reset(1),.in3(di3),.in2(di2),.in1(di1),.in0(di0),.an(an0),.a(a0),.b(b0),.c(c0),.d(d0),.e(e0),.f(f0),.g(g0));

endmodule

module roll(

input [3:0] in7,

input [3:0] in6,

input [3:0] in5,

input [3:0] in4,

input [3:0] in3,

input [3:0] in2,

input [3:0] in1,

input [3:0] in0,

input clk,

input reset,

output reg [3:0] d7,

output reg [3:0] d6,

output reg [3:0] d5,

output reg [3:0] d4,

output reg [3:0] d3,

output reg [3:0] d2,

output reg [3:0] d1,

output reg [3:0] d0

);

reg [29:0] count;

parameter maxcount = 100000000;

//parameter maxcount = 10;

reg clk\_2s;

// 生成 2s 时钟信号

always @(posedge clk or posedge reset) begin

if (reset) begin

clk\_2s <= 0;

count <= 0;

end else if (count < maxcount) begin

count <= count + 1;

end else if (count == maxcount) begin

count <= 0;

clk\_2s <= ~clk\_2s;

end

end

reg [3:0] state;

always @(posedge clk\_2s or posedge reset) begin

if (reset) begin

state <= 0;

end else if(state==7) state<=0;

else begin

state <= state + 1;

end

end

always @(\*) begin

case (state)

3'b000: begin

d7 = in7;

d6 = in6;

d5 = in5;

d4 = in4;

d3 = in3;

d2 = in2;

d1 = in1;

d0 = in0;

end

3'b001: begin

d7 = in6;

d6 = in5;

d5 = in4;

d4 = in3;

d3 = in2;

d2 = in1;

d1 = in0;

d0 = in7;

end

3'b010: begin

d7 = in5;

d6 = in4;

d5 = in3;

d4 = in2;

d3 = in1;

d2 = in0;

d1 = in7;

d0 = in6;

end

3'b011: begin

d7 = in4;

d6 = in3;

d5 = in2;

d4 = in1;

d3 = in0;

d2 = in7;

d1 = in6;

d0 = in5;

end

3'b100: begin

d7 = in3;

d6 = in2;

d5 = in1;

d4 = in0;

d3 = in7;

d2 = in6;

d1 = in5;

d0 = in4;

end

3'b101: begin

d7 = in2;

d6 = in1;

d5 = in0;

d4 = in7;

d3 = in6;

d2 = in5;

d1 = in4;

d0 = in3;

end

3'b110: begin

d7 = in1;

d6 = in0;

d5 = in7;

d4 = in6;

d3 = in5;

d2 = in4;

d1 = in3;

d0 = in2;

end

3'b111: begin

d7 = in0;

d6 = in7;

d5 = in6;

d4 = in5;

d3 = in4;

d2 = in3;

d1 = in2;

d0 = in1;

end

default: begin

d7 = in7;

d6 = in6;

d5 = in5;

d4 = in4;

d3 = in3;

d2 = in2;

d1 = in1;

d0 = in0;

end

endcase

end

endmodule

module display(

input clk,

input reset,

input [3:0]in3,

input [3:0]in2,

input [3:0]in1,

input [3:0]in0,

output [3:0]an,

output a,

output b,

output c,

output d,

output e,

output f,

output g

);

wire [1:0]pick;

wire [3:0]out;

clk\_div clk\_div1(.clk(clk),.reset(~reset),.pick(pick));

select select1(.in3(in3),.in2(in2),.in1(in1),.in0(in0),.pick(pick),.an(an),.out(out));

pin pin1(.din(out),.a(a),.b(b),.c(c),.d(d),.e(e),.f(f),.g(g));

endmodule

module clk\_div(

input clk,

input reset,

output reg[1:0] pick

);

reg [19:0]count;

parameter maxcount=100000;

//parameter maxcount = 10;

reg clk\_2ms;

always@(posedge clk or posedge reset)

begin

if(reset) begin clk\_2ms<=0;count<=0;end

else if(count<maxcount) count<=count+1;

else if(count==maxcount) begin count<=0;clk\_2ms<=~clk\_2ms;end

end

always@(posedge clk\_2ms or posedge reset)

begin

if (reset) begin pick<=3;end

else if(pick==0) pick<=3;

else pick<=pick-1;

end

endmodule

module select(

input [3:0] in3,

input [3:0] in2,

input [3:0] in1,

input [3:0] in0,

input [1:0] pick,

output reg [3:0] an,

output reg [3:0] out

);

always @(\*) begin

case(pick)

2'b00: out = in0;

2'b01: out = in1;

2'b10: out = in2;

2'b11: out = in3;

default: out = 4'b0000;

endcase

an[0]=~pick[1] & ~pick[0];

an[1]=~pick[1] & pick[0];

an[2]=pick[1] & ~pick[0];

an[3]=pick[1] & pick[0];

end

endmodule

module pin(

input [3:0]din,

output reg a,

output reg b,

output reg c,

output reg d,

output reg e,

output reg f,

output reg g

);

always @(\*) begin

case(din)

4'b0000 : {a,b,c,d,e,f,g}=7'b1111110;

4'b0001 : {a,b,c,d,e,f,g}=7'b0110000;

4'b0010 : {a,b,c,d,e,f,g}=7'b1101101;

4'b0011 : {a,b,c,d,e,f,g}=7'b1111001;

4'b0100 : {a,b,c,d,e,f,g}=7'b0110011;

4'b0101 : {a,b,c,d,e,f,g}=7'b1011011;

4'b0110 : {a,b,c,d,e,f,g}=7'b1011111;

4'b0111 : {a,b,c,d,e,f,g}=7'b1110000;

4'b1000 : {a,b,c,d,e,f,g}=7'b1111111;

4'b1001 : {a,b,c,d,e,f,g}=7'b1111011;

default : {a,b,c,d,e,f,g}=7'b1111110;

endcase

end

endmodule